KESTREL-V: A Secure RISC-V System-on-Chip for Trusted eBPF Hardware Acceleration

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September 3, 2025

Abstract

The increasing demand for programmable, high-performance networking in AI and HPC fabrics necessitated a move beyond fixed-function hardware. eBPF (extended Berkeley Packet Filter) has emerged as the standard for such programmability, but software-based execution remains a bottleneck. This paper introduces KESTREL-V, a System-on-Chip (SoC) that implements the eBPF ISA directly in hardware. By integrating 8 isolated hardware VM slots within a Trusted Execution Environment (TEE), KESTREL-V enables wire-speed, verifiable packet processing at exascale without host CPU overhead.

1 Introduction

Modern data center networking requires extreme flexibility and security. Traditional network interface cards (NICs) often lack the programmability needed for evolving AI workloads, while software-based solutions introduce prohibitive latency. KESTREL-V (Keystone Enclave Secured TRusted eBPF Logic on RISC-V) addresses this by providing a hardware-accelerated platform for eBPF execution, integrated into a RISC-V SoC architecture.

2 System Architecture

The KESTREL-V SoC is built upon an open and modular architecture centered on a 64-bit RISC-V CVA6 application-class core. The system utilizes a high-performance AXI4 interconnect to manage data flow between the main processor, memory, and the specialized Keystone Coprocessor.

2.1 Custom ISA Extensions

To achieve seamless integration, the CVA6 core implements a custom "Y" ISA extension. This extension provides direct hardware instructions for managing eBPF VM lifecycles, status monitoring, and low-latency data passing via secure mailboxes, bypassing traditional interrupt-driven overheads.

3 The Keystone Coprocessor

The core innovation of KESTREL-V is the Keystone Coprocessor. It acts as an autonomous hardware accelerator capable of offloading entire eBPF programs from the primary CPU.

3.1 Hardware VM Slots

The coprocessor features eight identical eBPF VM slots. Each slot is a hardware-hardened execution environment containing:

- **PicoRV32 Nano-controller**: A compact RISC-V core optimized for eBPF interpretation.
- **Isolated Memories**: Dedicated program and stack RAM for each VM, ensuring multi-tenant security.
- **DMA Engine**: A shared high-speed AXI master port for loading programs directly from main memory.

4 Security and Trusted Execution

KESTREL-V is designed for multi-tenant AI clusters where security is paramount. The TEE enclave-secured logic ensures that eBPF programs are isolated from the host operating system and hypervisor. Remote attestation guarantees that only verified, unmodified code is executed within the hardware VMs.

5 Application in AI/HPC Fabrics

By offloading complex network functions—such as RDMA/RoCE header manipulation and MPI col-

lective operations—directly to silicon, KESTREL-V enables deterministic, wire-speed performance critical for high-bandwidth AI fabrics.

6 Conclusion

KESTREL-V represents a significant leap forward in disaggregated, programmable hardware. By marrying the flexibility of eBPF with the openness of RISC-V, PacketFive provides a foundation for the next generation of trusted, high-performance networking infrastructure.